IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	
Jonathan E. Greene	Confirmation No.: 3585
Application No.: 10/643,164	Art Unit: 2124
Filed: August 18, 2003	Examiner: C. C. Do
For: METHODS AND APPARATUS FOR FAST FOURIER TRANSFORMS	

APPEAL BRIEF

MS Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Applicant-Appellant appeals to the Board of Patent Appeals and Interferences (the "Board") from the Examiner's rejection of pending claims 60-61 of the above-cited application. A notice to this effect was filed on April 2, 2007. Pursuant to 37 C.F.R § 41.37(a), fees in the amount of $250.00 are filed herewith. Please charge any additional fees to Deposit Order Account 14-1449.

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REAL PARTY IN INTEREST

The real party in interest in this appeal is Mercury Computer Systems, Inc., a Massachusetts corporation having a principal place of business in Chelmsford, Massachusetts.

RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 1 – 59 have been cancelled.[1]

Claims 60 – 61 stand rejected. It is the rejection of these claims that the Applicants appeal. Claims 60 – 61 are reprinted in Appendix A, hereof.

[1] Cancelled claims 1 – 46 previously issued in Parent application no. 09/728,469, now, U.S. Patent No. 6,609,140.

STATUS OF AMENDMENTS

Claim 60 was amended in a Response filed on March 5, 2007, subsequent to the Final Office Action mailed on January 4, 2007. The amendments were entered by the Examiner, as reflected in the Advisory Action dated March 21, 2007. The claims listed in Appendix A reflect those amendments.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 60 recites a computer system that utilizes hardware (i.e., vector processors) to generate a series of coefficient values (i.e., butterfly calculation outputs) without the need for additional processing (i.e., without an additional bit-reversal ordering pass).

Specifically, the claimed invention is directed to a computer system for performing a Fast Fourier transform on N ordered inputs in n stages.[2] The system includes one or more vector processors configured as a non-final stage calculating means for repetitively performing in-place butterfly calculations for n–1 stages.[3] The one or more vector processors are further configured as a final stage calculating means for performing a final stage of butterfly calculations.[4] The final stage includes a first loop means for performing a portion of the final stage butterfly calculations, and a second loop means for performing a remaining portion of the final stage butterfly calculations.[5]

The first loop means performs a set of butterfly calculations, and stores outputs therefrom in shuffled order in place of selected inputs to result in a correct ordering of transform outputs.[6] The second loop means performs two sets of butterfly calculations, and stores outputs from the

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[2] *See, e.g.,* specification at page 7, line 11 – page 8, line 7.

[3] *See, e.g.,* specification at page 7, line 28 – page 9, line 9; figure 1, elements 16; page 16, lines 12 – 16.

[4] *See, e.g.,* specification at page 9, lines 10 – 16; figure 1, element 18; page 16, lines 12 – 16.

[5] *See, e.g.,* specification at page 5, line 12 et. seq.

[6] *See, e.g.,* specification at page 5, lines 12-18; page 10, line 18 et seq.; element 22 of Figure 1; Figure 2; Appendix to Specification (added by way of amendment filed this day herewith) on page 22, line beginning **while (scnt)** … through page 26, line ending **/*end butterfly loop*/**

first set of those calculations in shuffled order in place of the inputs selected for the second set of those calculations. [7] Conversely, it stores butterfly calculation outputs from the second set in shuffled order in place of inputs selected for the first set to result in a correct ordering of transform outputs.[8] The final stage calculating means performs all butterfly calculations as radix-4 butterflies having four inputs and four outputs.[9]

In further accord with the claim, N is defined a power of two,[10] and the non-final stage calculating means is recited as performing a first stage of radix-8 butterfly calculations followed by $n - 2$ stages of radix-4 butterfly calculations.[11]

The computer system produces the correct ordering of transform outputs with no need to perform an additional bit-reversal ordering pass.[12]

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[7] *See, e.g.,* specification at page 5, lines 20-27; page 13 et seq.; element 24 of Figure 1; Figure 4; Appendix to Specification (added by way of amendment filed this day herewith) on page 26, line beginning **bflycnt = index >> 4** through page 29, line ending **/*end butterfly loop*/**

[8] *Id.*

[9] *See, e.g.,* specification at page 10, line 10.

[10] *See, e.g.,* specification at page 8, line 7; Appendix to Specification (added by way of amendment filed this day herewith) on page 13 at the line beginning **N = 1 << LOG2N**

[11] *See, e.g.,* specification at page 8 line 30 – page 9 line 1; Appendix to Specification (added by way of amendment filed this day herewith) on page 13, line beginning **if (LOG2N & 1)** through page 15, line ending **/*end radix-8 first pass*/**

[12] *See, e.g.,* specification at page 5, lines 1-6.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issue presented for review in this appeal is whether independent claim 60 and dependent claim 61 are directed to statutory subject matter as required under 35 U.S.C. §101.

ARGUMENT

Claim 60 Provides a Useful, Concrete and Tangible Result

A claim is statutory if it provides a "useful, concrete, and tangible result," even if that result is merely a set of numbers. *State St. Bank & Trust Co. v. Signature Fin. Group*, 149 F.3d 1368, 1375 (Fed. Cir. 1998), *citing In re Alappat*, 33 F.3d 1526, 1544, 31 U.S.P.Q.2D (BNA) 1545, 1557. Claim 60 meets — and, indeed, exceeds — this requirement. As such, if falls well the strictures of 35 U.S.C. §101 and should be allowed.

Claim 60 recites a computer system that uses hardware components (i.e., vector processors) to generate a series of values (i.e., butterfly calculation outputs) representing values of coefficients, without need for additional processing (i.e., an additional bit-reversal ordering pass). This compares favorably, from the perspective of 35 U.S.C. 101, with claims that the Court found patentable in *Alappat*; *Arrhythmia Research Technology Inc. v. Corazonix Corp.*, 958 F.2d 1053, 22 U.S.P.Q.2D (BNA) 1033 (Fed. Cir. 1992); and, *State St. Bank & Trust Co.:*

> In Alappat, we held that data, transformed by a machine through a series of mathematical calculations to produce a smooth waveform display on a rasterizer monitor, constituted a practical application of an abstract idea (a mathematical algorithm, formula, or calculation), because it produced "a useful, concrete and tangible result" — the smooth waveform.
>
> Similarly, in *Arrhythmia Research Technology Inc. v. Corazonix Corp.*, 958 F.2d 1053, 22 U.S.P.Q.2D (BNA) 1033 (Fed. Cir. 1992), we held that the transformation of electrocardiograph signals from a patient's heartbeat by a machine through a series of mathematical calculations constituted a practical application of an abstract idea (a mathematical algorithm, formula, or calculation), because it corresponded to a useful, concrete or tangible thing — the condition of a patient's heart.

> Today, we hold that the transformation of data, representing discrete dollar amounts, by a machine through a series of mathematical calculations into a final share price, constitutes a practical application of a mathematical algorithm, formula, or calculation, because it produces "a useful, concrete and tangible result" — a final share price momentarily fixed for recording and reporting purposes and even accepted and relied upon by regulatory authorities and in subsequent trades.

State St. Bank & Trust Co., supra, 149 F.3d at 1373.

More particularly, for example, in *Alappat*, the Federal Circuit held that a claim directed to a machine that converts data representing sample magnitudes of an input waveform, via mathematical operations, into pixel illumination intensity data is statutory subject matter under §101. *Alappat*, 33 F.3d at 1544-1545. The Court reasoned that the claim was directed to a machine, which is one of the four categories of patentable subject matter, and hence it appeared on its face to be directed to §101 subject matter. *Id.* at 1544. Further, the claim did not recite a "disembodied mathematical concept which may be characterized as an 'abstract idea,' but rather a specific machine to produce a useful, concrete, and tangible result." *Id.* In particular, the Court noted that the pixel illumination data could be used to produce a smooth waveform display. *Id.* The Court emphasized that "[T]he fact that the four claimed means elements function to transform one set of data to another through what may be viewed as a series of mathematical calculations does not alone justify a holding that the claim as a whole is directed to nonstatutory subject matter." *Id.*

Similarly, by way of further example, in *State Street Bank,* the Federal Circuit held that "the transformation of data, representing discrete dollar amounts, by a machine through a series of mathematical calculations into a final share price, constitutes a practical application of a mathematical algorithm, formula, or calculation, because it produces "a useful, concrete and

tangible result"— a final share price momentarily fixed for recording and re porting purposes and even accepted and relied upon by regulatory authorities and in subsequent trades." *State St. Bank & Trust Co., supra,* at 1373.

Like the claims at issue in *Alappat* and *State Street Bank*, Applicants' claimed invention is directed to a machine, in the form of a system comprising a plurality of vector processors, that *inter alia* generates a series of values (i.e., butterfly calculation outputs) representing coefficients without need for additional processing (i.e., without an additional bit-reversal ordering pass). More specifically, as in *Alappat* and *State Street Bank,* claim 60 recites specific structures (vector processors, in the case of claim 60; processing means in the form of arithmetic logic circuits, in *Alappat* and *State Street Bank*) that transform one set of data (ordered inputs, in the case of claim 60; sample magnitudes of an input waveform, in *Alappat*; and, discrete dollar amounts, in *State Street Bank*) into a tangible and useful output (ordered outputs, in the case of claim 60; pixel illumination intensity data in *Alappat*; and final share price in *State Street Bank*).

Consistent with the case law, the United States Patent and Trademark Office's own Manual of Patent Examining Procedure (MPEP) provides:

> ...USPTO personnel shall review the claim to determine it produces a useful, tangible, and concrete result. In making this determination, the focus is not on whether the steps taken to achieve a particular result are useful, tangible, and concrete, but rather on whether the final result achieved by the claimed invention is "useful, tangible, and concrete."

MPEP 2106(IV)(C)(2)((2)).

Claim 60 comports with this guideline as the final result, namely, the outputs, are useful, tangible, and concrete. Moreover, following the guidelines enumerated in this section of the

MPEP, the result is concrete as it is predictable and repeatable (MPEP 2106(IV)(C)(2)((2))(c)). Each time the claimed invention is used, it will produce ordered transform outputs. The result is tangible as it is a real world result (MPEP 2106(IV)(C)(2)((2))(b)) in the form of outputs that are ordered. The result is also useful in that the ordered outputs are specific, substantial, and credible (MPEP 2106(IV)(C)(2)((2))(a)). The ordering of the outputs allows them to used with any additional post-processing of the outputs, as described in the Applicant's specification on page 5.

For these reasons alone, claim 60 is statutory under 35 U.S.C. 101, and the Examiner's rejection should withdrawn. However, there is more . . .

Claim 60 Recites Physical Stucture

According to the Manual of Patent Examining Procedure, a claim defines statutory subject matter if it identifies the physical structure of a machine in terms of hardware or hardware and a software. Claim 60 does that. For this reason, too, it is patentable under 35 U.S.C. 101.

More specifically, MPEP 2106(IV)(B)(2)(a) provides:

> If a claim defines a useful machine or manufacture by identifying the physical structure of the machine or manufacture in terms of its hardware or hardware and software combination, it defines a statutory product. See, e.g., *Lowry*, 32 F.3d at 1583, 32 USPQ2d at 1034-35; *Warmerdam*, 33 F.3d at 1361-62, 31 USPQ2d at 1760.

Claim 60 comports with the above guideline as it defines a computer system that includes specific hardware structures, namely, vector processors. Moreover, it defines those structures in

connection with *means* (implemented in software), namely, the *first loop means, second loop means, non-final stage caclulating means,* and *final stage calculating means* that are implemented, in the specification, in software. *See,* the Summary of Claimed Subject Matter, *supra.*

As known in the art, a vector processor is a piece of hardware that is able to run mathematical operations on multiple data elements simultaneously. See uncontested definition of *vector processor* submitted by Applicants in Response to Office Action, filed November 6, 2006, at p. 4. The vector processors recited in claim 60 are configured to execute a specific task so as to generate tangible results. More specifically, they are configured, via *non-final stage calculating means* and *final stage calculating means* to provide Fourier transform outputs, as discussed above.

For the foregoing reasons, too, claim 60 is statutory under 35 U.S.C. 101.

Claim 61

Claim 61 recites further features of the computer system of claim 60. For the reasons above, claim 61 is also patentable under 35 U.S.C. 101.

CONCLUSION

As discussed herein, recite statutory subject matter under 35 U.S.C. 101. The Applicant-Appellant respectfully requests that the Board hold thusly and reverse the Examiner's rejections.

Respectfully submitted,

Dated: /August 2, 2007/

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APPENDIX A – CLAIMS APPENDIX

60. A computer system for performing a fast Fourier transform on N ordered inputs in n stages comprising:

one or more vector processors configured as a non-final stage calculating means for repetitively performing in-place butterfly calculations for n–1 stages;

the one or more vector processors further configured as a final stage calculating means for performing a final stage of butterfly calculations including:

a first loop means for performing a portion of the final stage butterfly calculations, the first loop means performing a set of butterfly calculations, and storing butterfly calculation outputs in shuffled order in place of the selected inputs to result in a correct ordering of transform outputs; and

a second loop means for performing a remaining portion of the final stage butterfly calculations, the second loop means performing two sets of butterfly calculations, and storing butterfly calculation outputs from a first one of the two sets of butterfly calculations in shuffled order in place of the inputs selected for a second one of the two sets of butterfly calculations and storing butterfly calculation outputs from the second one of the two sets of butterfly calculations in shuffled order in place of the inputs selected for the first one of the two sets of butterfly calculations to result in a correct ordering of transform outputs,

wherein the final stage calculating means performs all butterfly calculations as radix-4 butterflies having four inputs and four outputs,

wherein N is a power of two, and

wherein the non-final stage calculating means performs a first stage of radix-8 butterfly calculations followed by n-2 stages of radix-4 butterfly calculations,

wherein the computer system produces the correct ordering of transform outputs with no need to perform an additional bit-reversal ordering pass.

61. The computer system of claim 60, wherein the non-final and final stage calculating means include a four-fold single instruction multiple data (SIMD) processor for performing four radix-4 butterfly calculations at a time.

APPENDIX B – EVIDENCE APPENDIX

No evidence is relied upon by Applicant-Appellant in this appeal, except the definition of *vector processor* submitted by Applicants in their Response to Office Action, filed November 6, 2006, at p. 4, excerpted below. That definition was uncontested in the proceedings herein:

Warmerdam, 33 F.3d at 1361-62, 31 USPQ2d at 1760.

Claim 60 comports with the above guideline as it defines a "machine" that includes spe hardware structures, namely, vector processors. As known in the art, a vector processor is a pie *hardware* that is able to run mathematical operations on multiple data elements simultaneously. *Wikipedia*, http://en.wikipedia.org/wiki/Vector_processor.

Further, the vector processors are configured to execute a specific task so as to generate

APPENDIX C – RELATED PROCEEDINGS APPENDIX

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.